What is claimed is:

1. A liquid crystal display of horizontal electric field applying type, which comprises:

a thin film transistor array substrate, comprising:

a gate line;

a common line parallel to the gate line;

a data line crossing the gate line and the common line with a gate insulating film therebetween to define a pixel area;

a thin film transistor formed on each intersection of the gate line and the data line;

a common electrode formed in the pixel area and connected to the common line;

a pixel electrode connected to the thin film transistor and formed to produce horizontal electric field along with the common electrode in the pixel area;

a gate pad formed with at least one conductive layer included in the gate line;

a data pad formed with at least one conductive layer included in the data line;

a common pad formed with at least one conductive layer included in the common line;

a passivation film exposing the gate pad, the data pad and the common pad, which are formed on a substrate to form the thin film transistor array substrate;

a color filter array combined with the thin film transistor array substrate, liquid crystal material being filled between the color filter and the thin film transistor array substrate; and

a conductive film connected to the gate pad, the data pad and the common pad, said pads exposed on the thin film transistor array substrate.

2. The liquid crystal display of horizontal electric field applying type of claim 1, wherein each of the gate line and the common line includes a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

3. The liquid crystal display of horizontal electric field applying type of claim 2, wherein each of the gate pad and the common pad comprise the main conductive layer and the subsidiary conductive layer, wherein the subsidiary conductive layer has an exposed structure.

4. The liquid crystal display of horizontal electric field applying type of claim 2, wherein each of the gate pad and the common pad includes the subsidiary conductive layer.

5. The liquid crystal display of horizontal electric field applying type of claim 2, wherein the main conductive layer includes at least one of an aluminum system metal, copper, molybdenum, chrome, tungsten, or low resistance metal, and wherein the subsidiary conductive layer includes a titanium.

6. The liquid crystal display of horizontal electric field applying type of claim 1, wherein the data line includes a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

7. The liquid crystal display of horizontal electric field applying type of claim 6, wherein each of the data pad includes the main conductive layer and the subsidiary conductive layer, wherein the subsidiary conductive layer has an exposed structure.

8. The liquid crystal display of horizontal electric field applying type of claim 6, wherein the data pad includes the subsidiary conductive layer.

9. The liquid crystal display of horizontal electric field applying type of claim 6, wherein the main conductive layer includes at least one of an aluminum system metal, copper, molybdenum, chrome, tungsten, or a low resistance metal, and wherein the subsidiary conductive layer includes titanium.

10. The liquid crystal display of horizontal electric field applying type of claim 1, wherein the liquid crystal display of horizontal electric field applying type further comprises an etching preventive layer for preventing the substrate from being etched.

11. The liquid crystal display of horizontal electric field applying type of claim 10, wherein the etching preventive layer includes a transparent oxide system material.

12. The liquid crystal display of horizontal electric field applying type of claim 10, wherein the etching preventive layer includes any one of TiO_2 and Al_2O_3.

13. The liquid crystal display of horizontal electric field applying type of claim 1, wherein the thin film transistor comprises:

a gate electrode connected to the gate line;

a source electrode connected to the data line;

a drain electrode opposite to the source electrode; and

a semiconductor layer overlapping with the gate electrode with the gate insulating film therebetween to form a channel portion between the source electrode and the drain electrode.

14. The liquid crystal display of horizontal electric field applying type of claim 13, wherein the drain electrode and the pixel electrode are made of an identical conductive layer.

15. The liquid crystal display of horizontal electric field applying type of claim 13, wherein the liquid crystal display of horizontal electric field applying type further comprises a storage capacitor, wherein the storage capacitor has a lower storage electrode formed by a portion of the common line and an upper storage electrode which is formed to overlap with the lower storage electrode and made of a conductive layer identical to that of the pixel electrode.

16. The liquid crystal display of horizontal electric field applying type of claim 15, wherein the semiconductor layer is formed on the gate insulating film along the data line, the source electrode, the drain electrode, the pixel electrode and the upper storage electrode.

17. The liquid crystal display of horizontal electric field applying type of claim 13, wherein the pixel electrode includes:

a finger part formed in parallel with the common electrode to produce the horizontal electric field along with the common electrode; and

a horizontal part connected to the finger part and formed in parallel with the gate line.

18. The liquid crystal display of horizontal electric field applying type of claim 17, wherein the semiconductor layer is formed to have a width identical to that of the finger part of the pixel electrode.

19. The liquid crystal display of horizontal electric field applying type of claim 18, the liquid crystal display of horizontal electric field applying type further comprises a passivation film for exposing the gate pad, the data pad, the common pad and the pixel electrode.

20. A method for fabricating a liquid crystal display of horizontal electric field applying type, which includes:

preparing a thin film transistor array substrate, wherein the thin film transistor array substrate includes a thin film transistor formed on a crossing of a gate line and a data line, a pixel electrode connected to the thin film transistor, a common electrode producing horizontal electric field along with the pixel electrode and a common line connected to the common electrode and wherein the thin film transistor array substrate has a gate pad formed with at least one conductive layer included in the gate line, a data pad formed with at least one conductive layer included in the data line and a common pad formed with at least one conductive layer included in the common line which are exposed through a passivation film;

preparing a color filter array substrate to be opposite to the thin film transistor array substrate;

combining the thin film array substrate and the color filter array substrate; and

connecting a conductive film to the gate pad, the data pad and the common pad.

21. The method of claim 20, wherein the step of preparing a thin film transistor array substrate includes:

forming on a substrate a first conductive pattern group having the gate line, a gate electrode of the thin film transistor, the common line parallel to the gate line, the common electrode, the gate pad and the common pad;

forming a gate insulating film on the substrate having the first conductive pattern group thereon;

forming a second conductive pattern group and a semiconductor layer having a channel of the thin film transistor and forming along the second conductive pattern

group, wherein the second conductive pattern group have the data line, a source electrode of the thin film transistor connected to the data line, a drain electrode of the thin film transistor being opposite to the source electrode, a pixel electrode connected to the drain electrode and paralleled to the common electrode and the data pad; and

forming a passivation film for exposing the gate pad, the data pad and the common pad on the gate insulation film having the second conductive pattern group and the semiconductor layer formed thereon.

22. The method of claim 21, wherein any one of the first and the second conductive pattern groups is formed to have a double-layer structure having a main conductive layer and a subsidiary conductive layer for providing against the opening of the main conductive layer.

23. The method of claim 22, wherein the step of forming the passivation film includes exposing subsidiary layers of the gate pad and the common pad.

24. The method of claim 22, wherein the step of forming the passivation film includes forming a contact hole passing through the passivation film and the gate insulation film to expose subsidiary layers of the gate pad and the common pad.

25. The method of claim 22, wherein the step of forming the passivation film includes forming a contact hole passing through the passivation film, the gate insulation film and main layers of the gate pad and the common pad to expose subsidiary layers of the gate pad and the common pad.

26. The method of claim 22, wherein the step of forming the passivation film includes exposing a subsidiary layer of the data pad.

27. The method of claim 22, wherein the step of forming the passivation film includes forming a contact hole passing through the passivation film to expose a subsidiary layer of the data pad.

28. The method of claim 22, wherein the step of forming the passivaion film includes forming a contact hole passing through the passivation film and a main layer of the data pad to expose a subsidiary layer of the data pad.

29. The method of claim 22, wherein the main layer includes at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten which are a low resistance metal, and wherein the subsidiary layer includes a titanium.

30. The method of claim 21, wherein the step of forming the second conductive pattern group further includes forming an upper storage electrode overlapped with the common line with the gate insulating film therebetween.

31. The method of claim 20, wherein the step of preparing the thin film transistor array substrate fruther includes:

preparing a substrate; and

forming an etching preventive layer on the substrate.

32. The method of claim 31, wherein the etching preventive layer includes a transparent oxide system material.

33. The method of claim 32, wherein the etching preventive layer includes any one of TiO_2 and Al_2O_3.

34. The method of claim 20, wherein said step of preparing the thin film transistor array substrate includes:

forming on a substrate a first conductive pattern group having the gate line, a gate electrode of the thin film transistor connected to the gate line, the common line parallel to the gate line, the common electrode, the gate pad and the common pad;

forming a gate insulating film on the substrate having the first conductive pattern group thereon;

forming the data line, a source electrode of the thin film transistor connected to the data line, a drain electrode of the thin film transistor opposite to the source electrode, a pixel electrode formed with at least one conductive layer included in the drain electrode and having a finger part to form a horizontal electric field along with the common electrode, a second conductive pattern group including the data pad and a semiconductor layer forming a channel portion of the thin film transistor and overlapped with the pixel electrode;

forming a passivation film on the gate insulating film so as to cover the semiconductor layer and the second conductive pattern group; and

patterning the semiconductor layer so that the finger part of the pixel electrode is formed to have a width identical to that of the pixel electrode.

35. The method of claim 34, wherein the step of forming the passivation film includes:

forming a contact hole passing through the passivation film to expose a subsidiary layer of the data pad, and

forming a contact hole passing through the passivation film and the gate insulating film to expose the semiconductor layer being overlapped with a subsidiary conductive layer of the pixel electrode and the pixel electrode.

36. The method of claim 22, wherein the step of forming the passivation film includes:

forming a contact hole passing through the passivation film and the main conductive layer to expose a subsidiary conductive layer of the data pad, and

forming a contact hole passing through the passivation film, the gate insulating film and the main conductive layer to expose the semiconductor layer being overlapped with a subsidiary conductive layer of the pixel electrode and the pixel electrode.

37. The method of claim 34, wherein the step of patterning the semiconductor layer includes dry-etching the semiconductor layer using a mask, the pixel electrode being employed as the mask.